HIGH SPEED AND EFFICIENT POWER REDUCTION IN PULSE TRIGGERED FLIPFLOP BASED ON SIGNAL FEED THROUGH SCHEME

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Abstract

Low power has emerged as a principal theme in today's electronics industry. The need for low power has caused a major paradigm shift where power dissipation has become as important a consideration as performance and area. So this Low Power Pulse Triggered Flip Flop reviews various strategies and methodologies for designing low power circuits and systems. In this paper an explicit type pulse-triggered structure and a modified true single phase clock latch based on a signal feed-through scheme is used. Pulse-triggered FF (P-FF) is a single- latch structure which is more popular than the conventional transmission gate (TG) and master– slave based FFs in high-speed applications.

Chapter 1
Introduction

Flip-flops (FFs) are the basic storage elements used extensively in all kinds of digital designs. In particular, digital designs now a-days often adopt intensive pipelining techniques and employ many FF-rich modules such as register file, shift register, and first in-first out. It is also estimated that the power consumption of the clock system, which consists of clock distribution networks and storage elements, is as high as 50% of the total system power. FFs thus contribute a significant portion of the chip area and power consumption to the overall system design. Pulse-triggered FF (P-FF), because of its single-latch structure, is more popular than the conventional transmission gate (TG) and master–slave based FFs in high-speed applications. Besides the speed advantage, its circuit simplicity lowers the power consumption of the clock tree system. A P-FF consists of a pulse generator for strobe signals and a latch for data storage. If the triggering pulses are sufficiently narrow, the latch acts like an edge-triggered FF. Since only one latch, as opposed to two in the conventional master–slave configuration, is needed, a P-FF is simpler in circuit complexity. This leads to a higher toggle rate for high-speed operations.

Chapter 2
Conventional flip-flop

P-FF's can be classified into two types, that is, implicit and explicit, depending on the implementation of pulse generator. In implicit type P-FF, the pulse generator is a built-in logic of the latch design, and no explicit pulse signals are generated. In explicit type P-FF, the designs of pulse generator and the latch are separate. Although implicit pulse generation is often considered as more power efficient, the lengthened signal discharge path in latch design leads to inferior timing characteristics. In design practices, one pulse generation circuitry can be shared among FFs within the same register in explicit pulse generation. This gives the explicit type designs advantages in both circuit complexity and power consumption. In this paper, we will therefore focus on the explicit type designs only.To provide a comparison, some existing P-FF designs are reviewed rst. Fig. (a) Shows a classic explicit P-FF design, named data-close to-output (ep-DCO) .

It contains a NAND-logic-based pulse generator and a semi dynamic true-single-phase-clock (TSPC) structured latch design. In this P-FF design, inverters I3 and I4 are used to latch data, and inverters I1 and I2 are used to hold the internal node X. The pulse width is determined by the delay of three inverters.

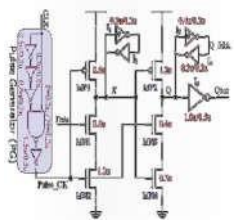
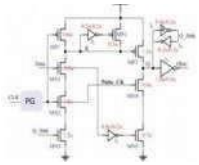


Fig (a)



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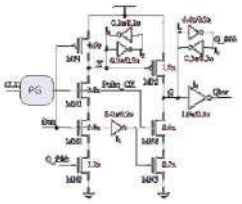

Fig (c)

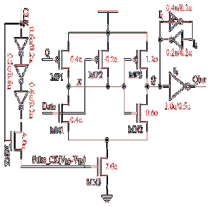

Fig (d)

Fig (a) ep-DCO (b) CDFF (c) Static CDFF (d) MHLFF

To overcome this problem, many remedial measures such as conditional capture, conditional precharge, conditional discharge, and conditional pulse enhancement scheme have been proposed. Fig. (b) shows a conditional discharged (CD) technique. An extra nMOS transistor MN3 controlled by the output signal Q_fdbk is employed so that no discharge occurs if the input data remains "1." In addition, the keeper logic for the internal node X is simpli ed and consists of an inverter plus a pull-up pMOS transistor only. The clock-gating in the conditional capture technique results in redundant power consumed by the gate controlling the de- livery of the delayed clock to the flip-flop. As a result, conditional precharge technique out performed the conditional capture technique in reducing the flip-flop EDP.But the conditional pre-charge technique has been applied only to ip-FF, and it is difficult to use a double-edge triggering mechanism for these flip-flops, as it will require a lot of transistors. A new technique, conditional discharge technique, is proposed in this chapter for both implicit and explicit pulse-triggered flip-flops without the problems associated with the conditional capture technique, Fig (b),Also, this new technique is employed to present a new flip-flop as well .In this technique, the extra switching activity is eliminated by controlling the discharge path when the input is stable HIGH and, thus the name Conditional Discharge Technique. In this scheme ,an nMOS transistor controlled by Qb is inserted in the discharge path of the stage with the high-switching activity. When the input undergoes a LOW-to-HIGH transition ,the output Q changes to HIGH and Qb to LOW. This transition at the output switches off the discharge path of the first stage to prevent it from discharging or doing evaluation in succeeding cycles as long as the input is stable HIGH. Fig (c) shows a similar P-FF design (SCDFF) using a static conditional discharge technique . It differs from the CDFF design in using a static latch structure. Node X is thus exempted from periodical precharges. It exhibits a longer data-to-Q (D-to-Q) delay than the CDFF design. Both designs face a worst case delay caused by a discharging path consisting of three stacked transistors, i.e., MN1–MN3.To overcome this delay for better speed performance, a powerful pull-down circuitry is needed, which causes extra layout area and power consumption. The modi ed hybrid latch ip- op (MHLFF) shown in Fig. (d) , also uses a static latch. The keeper logic at node X is removed.

A weak pull-up transistor MP1 controlled by the output signal Q maintains the level of node X when Q equals 0. Despite its circuit simplicity, the MHLFF design encounters two drawbacks. First, since node X is not predischarged, a prolonged 0 to 1 delay is expected. The delay deteriorates further, because a level-degraded clock pulse (deviated by one V)is applied to the discharging transistor MN3. Second, node X becomes oating in certain cases and its value may drift causing extra dc power

Chapter 3
Modified P-FF Design

Recalling the four circuits reviewed in Section 5.1, they all encounter the same worst case timing occurring at 0 to 1 data transitions. Referring to Fig. (a) to (e) , the proposed design adopts a signal feed-through technique to improve this delay.

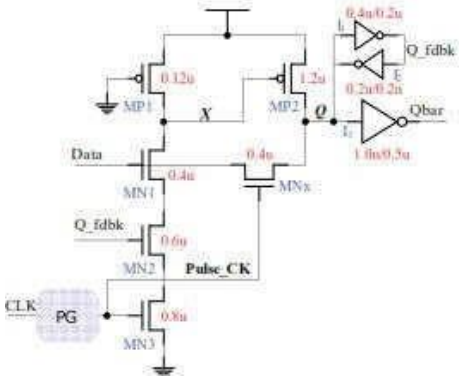

Fig (e) Modified circuit

Similar to the SCDFF design, the proposed design also employs a static latch structure and a conditional discharge scheme to avoid super uous switching at an internal node. However, there are three major differences that lead to a unique TSPC latch structure and make the proposed design distinct from the previous one. First, a weak pull-up pMOS transistor MP1 with gate connected to the ground is used in the rst stage of the TSPC latch. This gives rise to a pseudo-nMOS logic style design, and the charge keeper circuit for the internal node X can be saved. In addition to the circuit simplicity, this approach also reduces the load capacitance of node X. Second, a pass transistor MNx controlled by the pulse clock is included so that input data can drive node Q of the latch directly (the signal feed-through scheme). Along with the pull-up transistor MP2 at the second stage inverter of the TSPC latch, this extra passage facilitates auxiliary signal driving from the input source to node Q. The node level can thus be quickly pulled up to shorten the data transition delay. Third, the pull-down network of the second stage inverter is completely removed. Instead, the newly employed pass transistor MNx provides a discharging path. The role played by MNx is thus twofold, i.e., providing extra driving to node Q during 0 to 1 data transitions, and discharging node Q during “1” to “0” data transitions. Compared with the latch structure used in SCDFF design, the circuit savings of the proposed design include a charge keeper (two inverters), a pull-down network (two nMOS transistors), and a control inverter. The only extra component introduced is an nMOS pass transistor to support signal feed through. This scheme actually improves the “0” to “1” delay and thus reduces the disparity between the rise time and the fall time delays. In comparison with other P-FF designs such as ep-DCO, CDFF,and SCDFF, the proposed design shows the most balanced delay behaviors. The principles of FF operations of the proposed design are explained as follows.

When a clock pulse arrives, if no data transition occurs, i.e., the input data and node Q are at the same level, on current passes through the pass transistor MNx, which keeps the input stage of the FF from any driving effort. At the same time, the input data and the output feedback Q_fdbk assume complementary signal levels and the pull-down path of node X is off. Therefore, no signal switching occurs in any internal nodes. On the other hand, if a "0" to "1" data transition occurs, node X is discharged to turn on transistor MP2, which then pulls node Q high. Referring to Fig. 5.2.1, this corresponds to the worst case timing of the FF operations as the discharging path conducts only for a pulse duration. However, with the signal feed through scheme, a boost can be obtained from the input source via the pass transistor MNx and the delay can be greatly shortened. Although this seems to burden the input source with direct charging/discharging responsibility, which is a common pitfall of all pass transistor logic, the scenario is different in this case because MNx conducts only for a very short period. Referring to Fig. 2(c), when a "1" to "0" data transition occurs, transistor MNx is likewise turned on by the clock pulse and node Q is discharged by the input stage through this route. Unlike the case of "0" to "1" data transition, the input source bears the sole discharging responsibility. Since MNx is turned on for only a short time slot, the loading effect to the input source is not signi cant. In particular, this discharging does not correspond to the critical path delay and calls for no transistor size tweaking to enhance the speed. In addition, since a keeper logic is placed at node Q, the discharging duty of the input source is lifted once the state of the keeper logic is inverted.

Chapter 4
Proposed Design

The Proposed system which is similar to the modified circuit .It also employs a static latch structure and a conditional discharge scheme to avoid super uous switching at an internal node, which includes the inverter which furtherly reduces the power consumption . Layout of the proposed FF design with inverter shows in fig (f)

Chapter 5
Results and discussions

The performance of the proposed P-FF design is evaluated against existing designs through post-layout simulations.

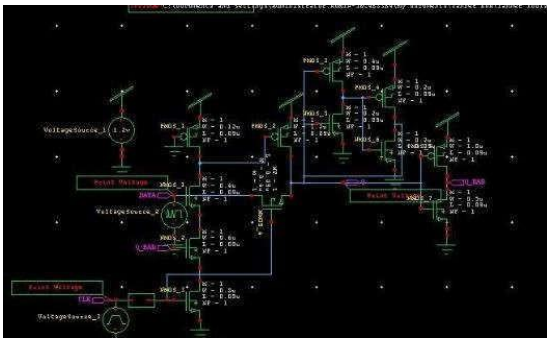

Fig (f) Layout of Proposed circuit with inverter

The compared designs include four explicit type P-FF designs shown in , an implicit type P-FF design named SDFF , a TG latch based P-FF design ep-SFF , plus two non-P-FF designs. One of them is a conventional TG master–slave-based FF (TGFF) and the other one is an adaptive-coupling-con gured FF design (ACFF) . A conventional CMOS NAND-logic-based pulse generator design with a three-stage inverter chain is used for all P-FF designs except the MHLFF design, which employs its own pulse generation circuitry as specie. The target technology is the TSMC 90-nm CMOS process. Since pulse width design is crucial to the correctness of data capture as well as the power consumption, the transistors of the pulse generator logic are sized for a design spec of 120 ps in pulse width in the TT case.

The sizing also ensures that the pulse generators can function properly in all process corners. With regard to the latch structures, each P-FF design is individually optimized subject to the product of power and D-to-Q delay. The operating condition used in simulations is 500 MHz/1.0 V. Six test patterns, each representing a different data switching probability, areapplied in simulations. Five of them are deterministic patterns, with 0% (all-0 or all-1), 12.5%, 25%, 50%, and 100% data transition probabilities, respectively.

FF Designs	ep-DCO	CDFF	SCDFF	MHLFF	Modified Ckt	Proposed
No. of Transistors	28	30	31	19	24	24
Layout Area	77.86	89.70	89.16	78.94	60.01	58.25
Min D to Q delay	118.9	129.5	140.0	173.8	106.1	103.0
Avg . Power	34.41	34.08	35.16	31.82	25.03	19.01

Feature comparison of various FF designs

Chapter 6
Conclusion

In this brief, we presented a novel P-FF design by employing a modified TSPC latch structure incorporating a mixed design style consisting of a pass transistor and pseudo-nMOS logic. The key idea was to provide a signal feedthrough from input source to the internal node of the latch, which would facilitate extra driving to shorten the transition time and enhance both power and speed performance. The design was intelligently achieved by employing a simple pass transistor. Extensive simulations were conducted, and the results did support the claims of the proposed design in various performance aspects.

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