Design and Application Verification of a Two-Stage Operational Amplifier using 90nm CMOS Technology

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ABSTRACT: Today VLSI technologies play the vital role and huge demand to design electronic circuits and systems with increasing miniaturization, portability, performance, reliability, and functionality. As Analog VLSI, the fundamental design is OP-AMP Integrated Circuits. Now a days, these OP-AMPs are most useful and most of the electronic devices are drastically used in signal conditioning, filtering and for execution of mathematical operations. Generally, two stage OP-AMPs preferred than single stage OP-amps because of enhanced gain, increased output swing, reduced noise, and improved bandwidth.

1. INTRODUCTION:

Operational amplifiers, commonly known as op-amps, play a crucial role in analog processing systems. In an ideal scenario, they function as voltage-controlled current sources with infinite voltage gain. Op-amps are vital components in numerous analog and mixed-signal systems. They are utilized in various levels of complexity to achieve functions ranging from DC bias generation to high-speed amplification or filtering. However, designing op-amps remains challenging due to the reduction in supply voltage and transistor channel lengths with each successive generation of CMOS technologies.

The progress in very large-scale integration (VLSI) technology has now reached a point where it is possible to integrate millions of transistors onto a single chip. Initially, integrated circuits were used as subsystem components, divided at analog-digital interfaces. Advancements in technology have reached a stage where it is feasible to integrate entire systems onto a single chip by merging analog and digital functions. Complementary Metal-oxide Semiconductor (CMOS) technology has gained substantial popularity in mixed-signal implementations owing to its capability to deliver high density and power efficiency in the digital domain, while simultaneously providing a suitable combination of components for analog design.

The operational amplifier (Op-Amp) needs to meet specific requirements concerning gain, stability, and operating frequency. To address the limitations of single-stage amplifiers, alternative architectures must be adopted. With the advancement of scaled processes, faster speeds are achievable, but this comes at the cost of lower open-loop gain and reduced voltage headroom, making it difficult to cascade multiple stages for higher gains. Multiple-stage amplifiers provide a viable approach to overcome the limitations imposed by power supply voltage and other

performance factors in single-stage amplifiers, allowing for higher gain circuit designs. Nonetheless, the implementation of multiple-stage amplifiers can be intricate, particularly concerning compensation. Two-stage operational amplifiers are frequently favored in multistage designs due to their ability to offer high gain and wide output swing. However, an uncompensated two-stage operational amplifier exhibits a two-pole transfer function, with both poles situated below the unity gain frequency, which can result in stability challenges.

2. ANALYSIS:

Two Stage Operational Amplifier consists 8 transistors M1 to M8 all are in saturation.

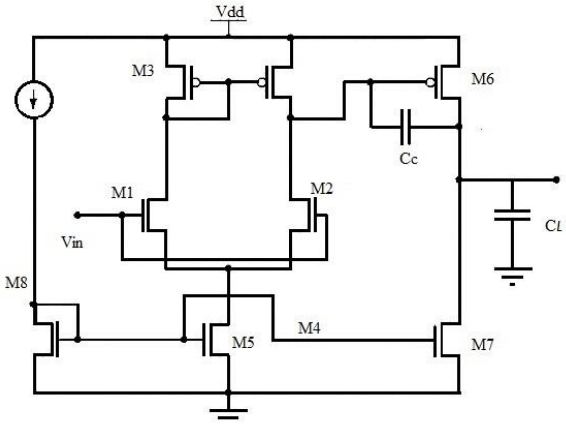

Figure 2.1 Circuit diagram of Two Stage Op-Amp.

In designing of op-amp, it has 12 steps to follow

- Select the smallest device length (L1 to L8) that ensures the channel length modulation parameter 'λ' is kept to a minimum.
- Compensation Capacitance 'C_C'

Given a target phase margin of $60^{0,}$ select the minimum value of the Compensation capacitor (C_C) required to achieve this phase margin.

$$\mathbf{C_C > 0.22 C_L}$$

- Tail Current $\mathbf{I_{D5}}$,we determine the minimum value for the tail current I_{D5} based on slew rate requirements.

$$\mathbf{I_{D5} = SR * C_C}$$

If SR (Slew Rate) is not given

$I_{D5} = 10 \log ((V_{DD} + |V_{SS}|) / 2T_s)$

where T_s is settling time

- Size of M_3PMOS transistor

$I_{D3} = ½ I_{D5}$; M_3 is in saturation

i.e., $I_{D5} = ½ \mu_p C_{ox} (W/L)_3 (V_{SG3} - |V_{th3}|)^2$

M_3 is diode connected, $V_{SG3} = V_{SD3}$

$I_{D3} = ½\ \mu_p C_{ox}(W/L)_3(V_{S3} - V_{G3} - |V_{th3}|)^2$

M_1 is in saturation

$V_{DS1} = V_{GS1} – V_{th1}$ Overdrive voltage

i.e.,$I_{D3} = \frac{1}{2}\mu_p C_{ox}(W/L)_3 [\ V_{DD} - |V_{th3}|_{max} - (V_{GS1} - |V_{th1}|)\ ]^2$

$(W/L)_3 = I_{D5} / [\ \mu_p C_{ox} [V_{DD} - |V_{th3}|_{max} - V_{in(max)} + |V_{th1}|]^2\ ]$

W/L of M_3 is determined by using maximum ICMR $[V_{in(max)}]$

$(W/L)_3 = (W/L)_4$ as M_3 and M_4 form current mirror

Ensure that the pole and zero resulting from Cgs3 and Cgs4 capacitances are not dominant by confirming that the pole P3 is greater than 10 times the unity-gain bandwidth (GB).

i.e., $P_3 = g_{m3}/ 2C_{gs3} > 10*GB$

where $C_{gs} = 2/3C_{ox}W/L$;

$g_{m3} = 2I_{D3}/ \mu_n C_{ox} (W/L)_3 (V_{SG3} - |V_{th3}|)$

- Size of M_5 NMOS transistor

Employing the minimum ICMR equation, compute V_{DS5} (sat) using the provided relation

$V_{DS5} = V_{in(min)} – V_{SS} – (I_{D5}/ (\mu_n C_{ox}(W/L)_1))^{1/2} –$ $V_{th1(max)}$ (overdrive voltage of M_5)

- Minimum ICMR equation is represented as

$V_{in(min)} = [I_{DS}/\beta_1] + V_{th1+}V_{DS5+}V_{th5} - I_{D5} - \frac{1}{2}[\mu_n C_{ox}(W/L)_5(V_{GS} - V_{th5})^2\ ]$

i.e., $(W/L)_5 = 2I_{D5} / \mu_n C_{OX} V_{DS5(sat)}$

- Size of M_6 PMOS transistor
- For reasonable phase margin (~60^0), the following relations should be satisfied.

$g_{m6} = 2.2\ g_{m4} (C_L/C_C)$

M_6 and M_4 have $V_{SG6} = V_{SG4}$

$g_{m6} >= 10g_{m1}$

$V_{SG4} = V_{SG6}$ gives

$(W/L)_6 = (W/L)_4 * (g_{m6}/g_{m4})$

- Calculation of I_D

I_{D5} can be evaluated by knowing g_{m6} and $(W/L)_6$

$g_{m6} = [2\mu_p C_{OX}(W/L)_6 I_{D6}]^{1/2}$

i.e., $g_{m6}^2 = 2\mu_p C_{OX}(W/L)_6\ I_{D6}$

$I_{D6} = g_{m6}^2 / 2\mu_p C_{OX}(W/L)_6$

- Size of M_7 PMOS transistor
  - $(W/L)_7 = (I_{D7}/I_{D5}) * (W/L)_5$

since $I_{D6}=I_{D7}$

- **Gain and Power dissipation**

Power dissipation check

$$P_{(dis)} = (V_{DD} + |V_{SS}|) * (I_{D6} + I_{D5})$$

Check if $P_{(dis)\ calculated} <= P_{(dis)\ desired}$

Gain specification check

$$A_V = g_{m2}\, g_{m6}\, (r_{o2}||r_{o4}) *(r_{o6}||r_{o7})$$

$$I_{D2} = I_{D4},\ r_{o2} = 1/\ \lambda_2 I_{D2},\ r_{o4} = 1/\ \lambda_4 I_{D4}$$

$$r_{o2}||r_{o4} = 1/\ (\ \lambda_2 I_{D2} + \lambda_4 I_{D4})$$

Since $I_{D2} = I_{D4}$

$$r_{o2}||r_{o4} = 1/I_{D2}(\lambda_2 + \lambda_4)$$

$$r_{o2}||r_{o4} = 2/I_{D5}(\lambda_2 + \lambda_4)$$

$$I_{D6}=I_{D7},\ \ r_{o6} = 1/\lambda_6 I_{D6}\ ,\ r_{o7} = 1/\lambda_7 I_{D7}$$

$$r_{o6}||\ r_{o7} = 1/\ (I_{D6}\lambda_6 + I_{D7}\ \lambda_7)$$

Since $I_{D6}=I_{D7}$, $\ r_{o6}||\ r_{o7} = 1/\ I_{D6}(\lambda_6 + \lambda_7)$

$$A_V\ = g_{m2} g_{m6} (r_{o2}||r_{o4}) *(r_{o6}||r_{o7})$$

$$A_V\ = 2g_{m2} g_{m6} * 1/\ [\ I_{D5}(\lambda_2 + \lambda_4) * I_{D5}(\lambda_6 + \lambda_7)]$$

Check if $A_{V\ calculated} > A_{V\ desired}$

3. RESULTS

Frequency Response :

In the frequency response shown in fig. we got a good gain over wide range of frequencies with high gain of around 65dB.We can observe that gainbandwidth product of nearly 30M Hz which provides a good gain over maximum of frequencies.

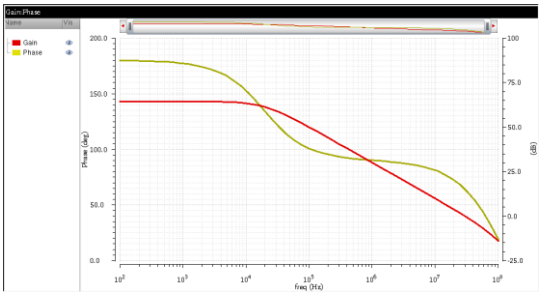

Figure 3.1. Gain & phase plot

Table 3.1: Parameters obtained after Simulation with V_{cm}=0.8V and 1.6V

PARAMETERS	VALUES	
	Vcm = 0.8V	**Vcm = 1.6V**
Supply	1.8 V	1.8 V

Channel Length	90nm	90nm
Load Capacitance	2pF	2pF
$\mu_n C_{ox}$	326.66µm	327.4 µm
$\mu_p C_{ox}$	171.28µm	171 µm
Gain	65.66 dB	64.23 dB
Slew Rate	20 V /µ.sec	20 V / µ.sec
UGF	28 M Hz	30 M Hz
3dB Bandwidth	16.47 K Hz	19.33 K Hz
Phase Margin	64 deg	63 deg
Power Dissipation	291 µW	316 µW

Table 3.2: W/L specifications of Op-Amp with V_{cm} = 1.6V.

MOSFET	W/L *in* μm
M_1, M_2	$3/0.5$
M_3, M_4	$7/0.5$
M_5, M_8	$6/0.5$
M_6	$87/0.5$
M_7	$37.5/0.5$

Parametric Analysis :

With respect to V_{cm}:

The change in gain, phase, and other parameters is analyzed with respect to variations in common mode voltage is shown in figure. In this we can deduce that gain, phase,bandwidth and unity gain frequency are almost remain same for various V_{cm} which suggests that design can be operated over wide range of input voltages with same performance.Only power dissipation increases minutely with V_{cm} .

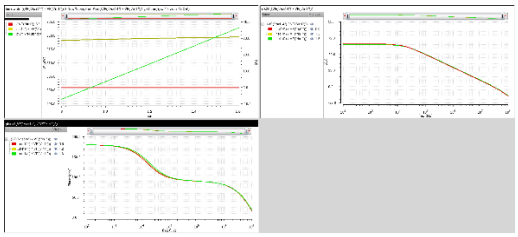

Figure 3.2 Parametric analysis with respect to V_{cm}

With respect to Cc:

The change in gain, phase, and other parameters is analyzed with respect to variations in coupling capacitance which acts as a feedback element is shown in figure. In this we can deduce that gain and phase various slightly for various Cc .Bandwidth remains same, unity gain frequency decreases

with increase in Cc and power dissipation decreases slightly at lower capacitances and become constant at higher frequencies.

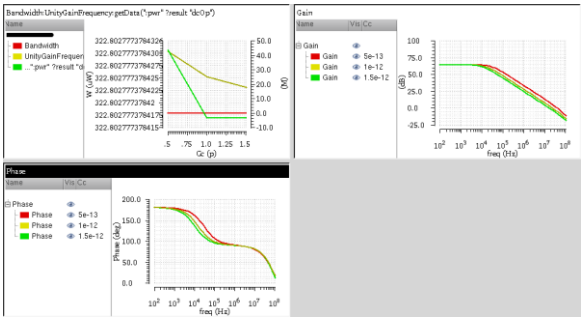

Figure 3.3 Parametric analysis with respect to C_c

With respect to C_L:

The change in gain, phase, and other parameters is analyzed with respect to variations in load capacitance which acts as a feedback element is shown in figure. In this we can deduce that gain and phase various slightly for various C_L at higher frequencies only .Bandwidth remains same, unity gain frequency decreases with increase in C_L and, power dissipation decreases slightly in micro watts at lower capacitances and become constant at higher frequencies.

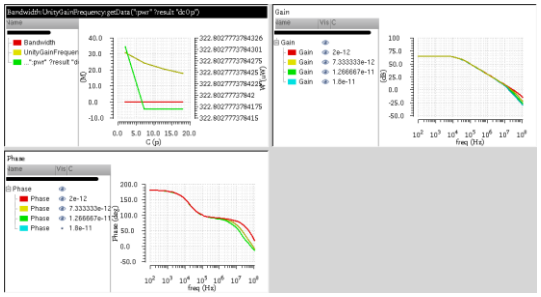

Figure 3.4. Parametric analysis with respect to C_L

4. APPLICATIONS:

Linear amplifiers such as op amps have many different applications. It has high open loop gain, high input impedance and low output impedance. It has a high common mode rejection r atio. Due to these favorable properties, it is used in various applications. In this article, we will disc uss some of the most important uses of op-amps

Adder:

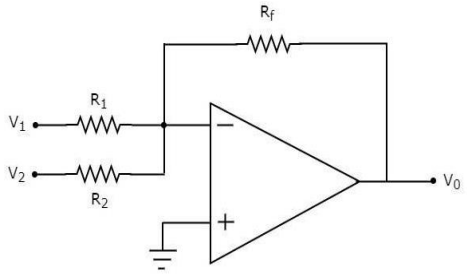

Figure 4.1. Circuit diagram of an op-amp based adder

$$V_0 = -R_f\left(\frac{V_1}{R_1} + \frac{V_2}{R_2}\right)$$

$$R_1 = R_2 = 8k\ ohm \qquad R_f = 16k\ ohm$$

$$= -2\ (V_1 + V_2)$$

Here we got an amplification factor of 2.

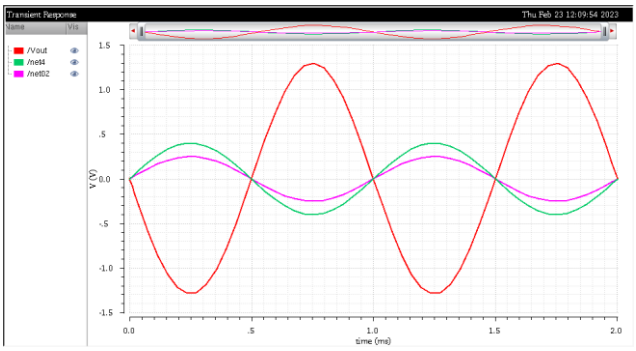

Figure 4.2. Gain plot of adder with gain

Subtractor:

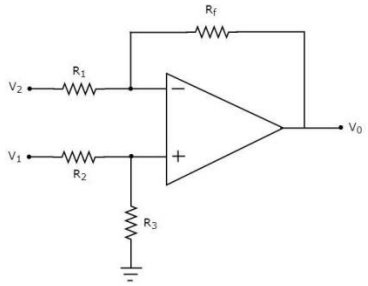

Figure 4.3. Circuit diagram of an op-amp based subtractor

$$V_0 = V_1\left(\frac{R_3}{R_2 + R_3}\right)\left(1 + \frac{R_f}{R_1}\right) - \frac{R_f}{R_1}V_2$$

$$if\ R_1 = R_2 = R_3 = 10k\ \ ;\ \ R_f = 100k;\ \mathrm{V_1} = 150\ \mathrm{mV},\ \mathrm{V_2} = 50\ \mathrm{mV}$$

On substituting above values in above equation we can get an output voltage of 325 mV with an amplification factor of 2.16.

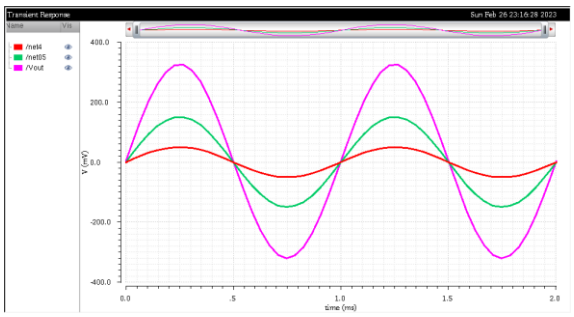

Figure 4.4. Transient Response of Subtractor with gain

Differentiator

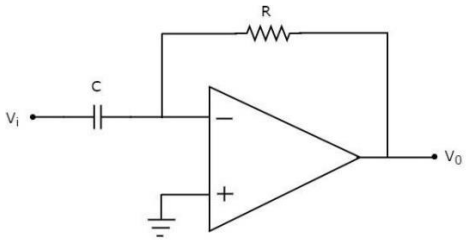

Fig 4.5. Circuit diagram of an op-amp based differentiator

$$V_0 = -RC\frac{dV_i}{dt}$$

$$R = 10k\ ohm, C = 1\ fF, V_i = 500\sin(2\pi \times 1000t)$$

On substituting above values in the equation we can get an output peak to peak voltage of $V_{pp} = 0.06\mu w$

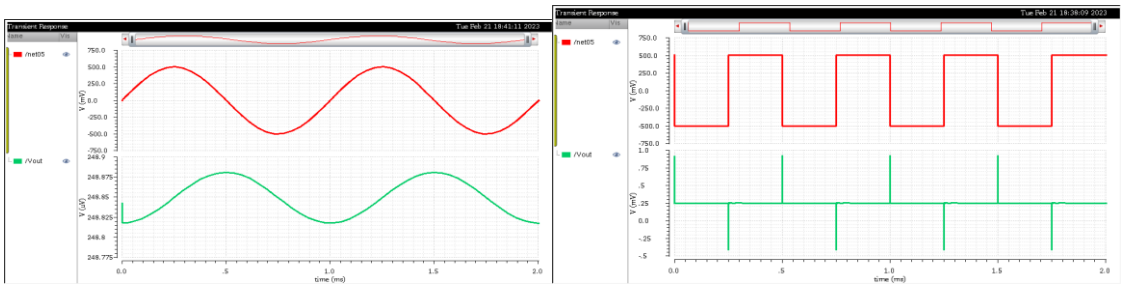

Figure 4.6. Sine and Square wave plot of differentiator

Integrator:

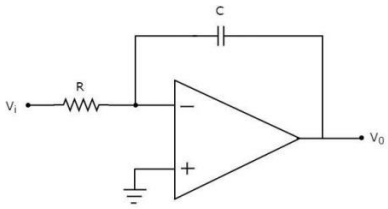

Figure 4.7. Circuit diagram of an op-amp based Integrator

$$V_0 = -\frac{1}{RC}\int V_i dt$$

$$V_i = 500sin(2\pi \times 1000t)\ \ mv$$

$$R = 8.5k\ ohm \qquad C = 10\ nF$$

On substituting above values in the equation and on integration we can get an output peak to peak voltage of $V_{pp} = 1.87V$.

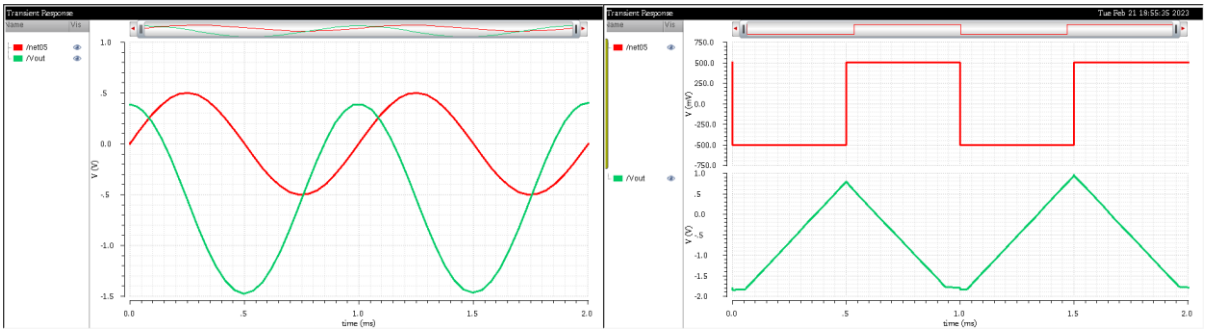

Figure 4.8 Sine and Square wave plot of Integrator

Buffer:

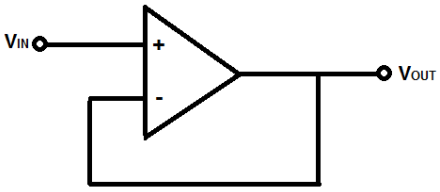

Figure 4.9. Circuit diagram of an op-amp based Buffer

Buffer acts as an element to separate points of two different impedances and passes input same to output.

V out=Vin.

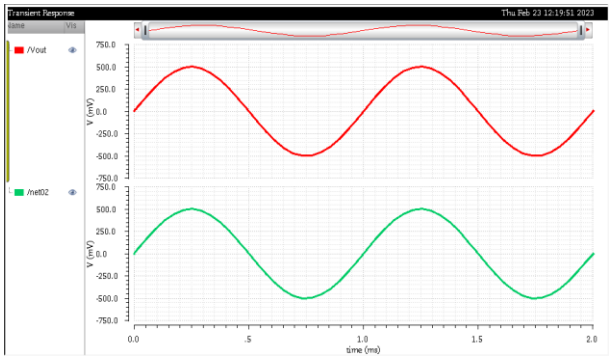

Figure 4.10. Transient Response of Buffer

5. CONCLUSION:

Table 5.1 shows comparison of this work with some references. If we consider ref [2], for same load capacitance of 2pF and power supply voltage of little higher we got increase in gain from 56.1 dB to 65.66dB and got low power dissipation of 291 µW, but decrease in phase margin from 77º to 64º and decrease in unity gain frequency.

Table 5.1: Comparison of Two stage Op-Amp Reference

PARAMETERS	Ref [2]	Ref [3]	Ref [4]
V_{cm}	-	-	0.9V

Power Supply	1V	3.3 V	1.8V
Channel Length	65nm	180nm	90nm
Load Capacitance	2pF	5pF	12pF
$\mu_n C_{ox}(A/v^2)$	-	-	320
$\mu_p C_{ox}(A/v^2)$	-	-	179
Gain(dB)	56.1	106.31	61
Slew Rate	-	3.87V/μs	18V/μs
Unity Gain Frequency	0.45GHz	48.62 MHz	30 MHz
3dB Bandwidth	-	198.1 Hz	-
Phase Margin	77º	57.53º	60º
Power Dissipation	1600 μW	685 μW	-

The design of a two-stage operational amplifier involves careful consideration of several key parameters such as gain, bandwidth, stability, and power consumption. Through a systematic design process that includes selecting appropriate transistor sizes, biasing schemes, and compensation techniques, it's possible to achieve a high-performance op-amp that meets the design requirements.

Overall, the design of a two-stage op-amp requires careful consideration of all the parameters and trade-offs involved, and it can be a challenging but rewarding process when done successfully. With the right design choices, a two-stage op-amp can provide high gain, low distortion, and stable operation for a wide range of applications.

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